

REMARKS

Claims 1-25 are pending in the application. Claims 1-5, 10-12, 14, and 17-25 were rejected, and claims 6-9, 13, 15, and 16 were objected to. Claims 10, 11, and 20 have been amended herein. In view of the claim amendments and the following remarks, reconsideration of the application is respectfully requested.

Title of the Invention Objection

The Examiner stated that the title of the invention was not descriptive, and required a new title. The proposed new title, "BUFFERED MEMORY MODULE SUPPORTING HIGH-SPEED SYSTEM MEMORY BUS USING WIDER MEMORY MODULE BUS", is more descriptive and supported by the specification, e.g., at page 5, lines 9-18.

Summary of the Invention Objection

The Office Action requested that Applicants add a "Summary of the Invention" description to the application. Applicants respectfully point out, however, that neither the MPEP nor 37 C.F.R. §1.73 requires the presence of a "Summary of the Invention." They merely indicate where in the application the "Summary of the Invention" should be placed when included. 37 C.F.R. §1.73 only states that a "Summary of the Invention" should be included. It does not state "must" or "shall." Accordingly, Applicants have elected not to include a "Summary of the Invention" as this is within the discretion and right of the Applicants.

Section 112 Rejection

Claim 20 was rejected under 35 U.S.C. § 112, as it was not clear what the value " M " represented in the claim. The value " M " was inadvertently deleted from the claim element "transferring the N data bits between the interface circuit and the R ranks of memory devices in \underline{M} $R \times m$ -bit-wide segments, where $M = \frac{N}{R \times m}$ is an integer value." Appropriate correction has now been effected. The correctness of the amended language is verifiable by substituting the value of " M " into the first clause and verifying that the result is an N -bit data transfer.

First Section (103)a Rejection

Claims 1-2, 4-5, and 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Raynham et al. (U.S. 6,530,033) and Canfield et al. (U.S. 5,825,424). Applicant respectfully traverses this rejection and submits that the combination of Raynham and Canfield does not present a prima facie case of obviousness for any of the rejected claims.

Claim 1

Applicant respectfully disagrees with the characterization of Canfield presented in the Office Action. As a first matter, regarding claim 1, Applicant can find no mention of a memory module and a module data bus in Canfield. Canfield describes unit 31 as an "adaptive decoder-memory interface" (col. 5, ll. 66-67), a "memory interface" (col. 6, ll. 1-2), and a "multiplexer" (col. 6, ll. 13). A single functional unit 31 is interposed between the processing units (30, 32) (and their internal system bus) and the entire external memory bus to all video frame memory 20, which strongly suggests the "memory interface" functions like a primary memory controller as claimed in claim 1, and not as a memory module interface circuit as claimed. This inference is bolstered by the teaching "[i]n this embodiment video frame memory 20 is located external to an integrated circuit which includes the MPEG decoder and associated elements 10-34 shown in Figure 1." (col. 4, ll. 37-39.) Thus Canfield's "internal memory bus" and "interface 31" are all part of the processing chip. Canfield's "internal memory bus" thus cannot be "coupled to the primary memory controller" as claimed, and Canfield's "interface 31" cannot be "an interface circuit" on a memory module as claimed.

Perhaps even more importantly, Canfield's memory interface 31 functions completely backwards when viewed against what appears in claim 1. Claim 1 recites at least one memory module "having a module data bus with an effective bit-width $N = R \times m$, where R is an integer value greater than one." In contrast, Canfield teaches "the internal memory bus data path [within Canfield's processor] is an integer multiple of the (external) memory bus data path." (col. 6, ll. 30-31, emphasis added.) Thus what is claimed, an effectively wider bus at the memory, is opposite of what Canfield teaches, a narrower bus at the memory.

Furthermore, the Examiner's suggested motivation for combining Canfield (to provide better memory management and data reduction by varying the data bit width of the external memory path as a function of the memory size) does not appear to be beneficial to Raynham, and thus applicant disagrees that such a motivation for combination exists. Raynham's application is for high-end servers with up to 64 GB of memory attached to a

wide memory bus (col. 12, ll. 42-60) with many memory modules. Canfield's application is for a low-cost MPEG decoder that can attach to relatively tiny amounts of memory (a maximum of 80 Mbits, easily available on a single SDRAM chip). Raynham's application seeks to deliver small memory system bandwidth and latency for large memory systems (col. 12, ll. 41-45), a goal that is not furthered by using less than all of the available data bit width. And in any event, such a combination does not result in the claim 1 invention.

Given that the references fail to teach or suggest all claim 1 elements, or suggest combination with each other, or any combination that falls within the scope of claim 1, Applicants respectfully submit that a prima facie case of obviousness is lacking in the combination.

Claim 2

In addition to the comments above, Applicants disagree with the Examiner's assertion that Raynham teaches the point-to-point bus as claimed. Raynham discloses a point-to-point segment to a central switch, and N memory modules "where each of the plurality of N memory modules is electrically connected radially to the central switch means by a separate memory module bus." (col. 5, ll. 36-50.) Thus Raynham's system has no "data bus segment connecting the primary memory controller and the first of the at least one memory modules" as claimed, since Raynham connects the primary memory controller only to a central switch. And Raynham's system has no additional segment "connecting the additional memory module to the module immediately preceding it" as claimed, since all modules connect to a central switch. The asserted combination thus fails to create a prima facie case of obviousness for claim 2.

Claim 4

In addition to the comments above regarding claim 1, Applicants disagree that Canfield teaches or suggests "the memory data bus clocking at a rate R times the clock rate of the module data bus" as recited in claim 4, where R is an integer value greater than 1 as stated in claim 1. The quotation relied on by the Examiner states the exact opposite: "the clock rate for the internal memory path is always less than the clock rate for the external memory path" (col. 6, ll. 29-33, emphasis added), assuming that one can even draw an analogy between Canfield's external memory data bus and a module data bus. The asserted combination thus fails to create a prima facie case of obviousness for claim 4.

Claim 5

As far as the comments above regarding claim 1 apply to a memory module, those same comments illustrate some of the reasons why a prima facie case of obviousness is

lacking for claim 5. Regarding the assertion that Canfield teaches a controller “capable of synchronizing the operation of the interface circuit and the memory device ranks” as claimed, Applicants must disagree since Canfield’s bus to memory (his external memory bus) is not taught to connect to multiple ranks in parallel, and thus cannot possible create one multiple-rank transfer wider than the external memory bus.

Claims 20 and 21

Applicants respectfully submit that a prima facie case of obviousness for claims 20 and 21 is lacking. Although claims 20 and 21 do not recite a controller, they do recite control functions for transferring data between a memory controller and a memory module. Accordingly, the remarks above regarding claim 5 are generally applicable as well regarding claims 20 and 21. Claim 20 adds the further concept, not found in the applied references, of M separate transfers of $R \times m$ -bit-wide segments to complete an N -bit transfer of data.

Claim 22

The Examiner is respectfully referred to the additional comments regarding claim 4 above, illustrating that Canfield fails to teach clocking between a memory controller and memory module at R times a module clock rate.

Second Section 103(a) Rejection

Claims 3, 10-12, and 17-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham et al. and Canfield et al. and in view of Osaka et al (U.S. 6,034,878). Applicant respectfully traverses this rejection and submits that the combination of Raynham, Canfield, and Osaka does not present a prima facie case of obviousness for any of the rejected claims. The Examiner is respectfully referred to the respective arguments above regarding the independent claims from which claims 3, 10-12, and 17-19 depend, as Osaka is not seen as detracting in any way from those arguments. Additionally, the following comments pertain directly to the limitations added by claims 3, 10-12, and 17-19 that do not appear in the prior art references used in the instant rejection.

Claim 3

Claim 3 recites a “ring data bus segment connecting the last of the memory modules in the memory system back to the primary memory controller”, within the point-to-point topology of claim 2. The references fail to teach or suggest such a limitation. Osaka teaches a standard multi-drop bus that happens to connect twice to the memory controller—this is not a segmented ring data bus, and does not suggest a segmented ring data bus.

Claims 10, 11, and 12

Claims 10-12 inadvertently referred back to claim 5, although claims 10 and 12 contain references to structure recited in claim 6 and should have referred back to that claim instead. Claims 10 and 11 have now been amended accordingly. Since the Examiner has indicated that claim 6 contains allowable subject matter, claims 10-12 are therefore allowable as well. Further, Applicants do not read the section of Osaka cited by the Examiner regarding claim 10 as having anything to do with clock rates—the section merely states that due to the loopback architecture of Osaka, timing does not change depending on which DRAM is addressed. Applicants further note that Osaka Figure 9 shows two data bus connection points at the top and bottom of a memory module, but not two sets of data signaling lines to two data registers.

Claims 17-19

The first section of Osaka cited by the Examiner (col. 10, ll. 39-43), to Applicants' understanding, refer to signals generated by a memory controller, and not to a "module further comprising a data strobe circuit to generate data strobe signaling when transmitting data over the memory data bus" as claimed in claim 17 or "when transmitting data from the interface circuit to the ranks of memory devices" as claimed in claim 19. The other sections of Osaka cited by the Examiner (col. 1, ll. 46-52; col. 13, ll. 39-42) refer to a system memory controller, and do not refer to an interface circuit as claimed in claims 18 and 19. In contrast, the "controller" recited in claim 18 is the memory module controller of claim 5, and responds to an externally-supplied data strobe signal, whereas Osaka's system memory controller does not. And the registers of Osaka are within his DRAM, not on a module that responds to data signaled and strobed from memory devices.

Objection to Allowable Claims

Claims 6-9, 13 and 15-16 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 23-25 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. In view of the arguments presented above for the patentability of the underlying base claims, and the amendment addressing the Section 112 rejection of claim 20, Applicant has elected not to rewrite these dependent claims at the present time.

Conclusion

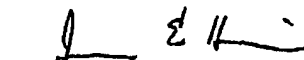
For the foregoing reasons, reconsideration and allowance of claims 1-25 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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PATENT TRADEMARK OFFICE

Respectfully submitted,

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